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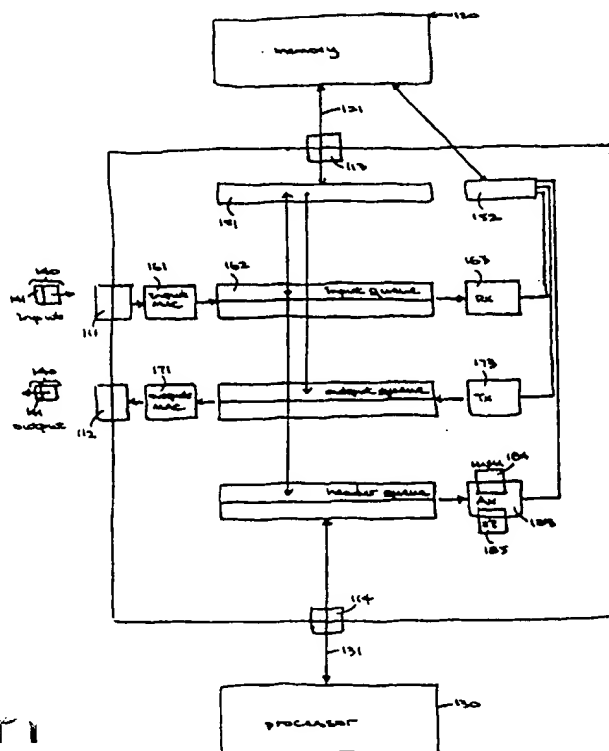
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(54) Title: SINGLE-CHIP ARCHITECTURE FOR SHARED-MEMORY ROUTER

(57) Abstract

The invention provides a single-chip method. The method includes a memory shared among packet buffers for receiving packets, packet buffers for transmitting packets, and packet header buffers for packet forwarding lookup. Accesses to that shared memory are multiplexed and prioritized. Packet reception is performed with relatively high priority, packet transmission is performed with medium priority, and packet forwarding lookup is performed with relatively low priority. The single-chip method includes circuits for serially receiving packet header information, converting that information into a parallel format for transmission to an SRAM for lookup, and queuing input packets for later forwarding at an output port. Similarly, the single-chip method includes circuits for queuing output packets for transmission at an output port, receiving packet forwarding information from the SRAM in a parallel format, and converting packet header information from output packets into a serial format for transmission. The single-chip method also includes a region in its shared memory for a packet forwarding table, and circuits for performing forwarding lookup responsive to packet header information.



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Title of the Invention

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Single-Chip Architecture For Shared-Memory Router

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This application claims priority of Provisional Application No. 60/060,628,  
hereby incorporated by reference as if fully set forth herein.

16

17

Background of the Invention

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19

*1. Field of the Invention*

20

21

22

This invention relates to a single-chip architecture for a shared-memory  
router.

1     2.     *Related Art*

2  
3             In a packet-switched network, a "router" is a device which receives pack-  
4     ets on one or more input interfaces and which outputs those packets on one of a plural-  
5     ity of output interfaces, so as to move those packets within the network from a source  
6     device to a destination device. Each packet includes header information which indi-  
7     cates the destination device (and other information), and the router includes routing in-  
8     formation which associates an output interface with information about the destination  
9     device (possibly with other information). The router can also perform other operations  
10    on packets, such as rewriting the packets' headers according to their routing protocol or  
11    to reencapsulate the packets from a first routing protocol to a second routing protocol.  
12

13            It is advantageous for routers to operate as quickly as possible, so that as  
14    many packets as possible can be switched in a unit time. Because routers are nearly  
15    ubiquitous in packet-switched networks, it is also advantageous for routers to occupy as  
16    little space as possible and to be easily integrated into a networking system. For exam-  
17    ple, implementing a router on a single chip (that is, a single integrated circuit) would be  
18    particularly advantageous.  
19

20            In this regard, one problem which has arisen in the art is that individual in-  
21    tegrated circuits and their packages are relatively limited in resources needed to imple-  
22    ment a router. In particular, individual chips have only a relatively limited number of  
23    pins, a relatively limited die area, and a relatively limited amount of power available for  
24    operation. These limitations severely limit the possibility of providing a useful router on  
25    a single chip. Routing devices generally need relatively more input and output ports

1 (thus requiring relatively more pins), relatively more lookup table space (thus requiring  
2 relatively larger die size for memory), relatively more packet buffering space (thus re-  
3 quiring relatively larger die size for memory), and relatively more packets routed in unit  
4 time (thus requiring relatively larger die size for processing ability and relatively larger  
5 power dissipation for speed).

6  
7 Accordingly, it would be advantageous to provide a single-chip router.  
8 This advantage is achieved in an embodiment of the invention in which a router inte-  
9 grated on a single chip shares memory among packet buffers for receiving packets,  
10 packet buffers for transmitting packets, and packet header buffers for packet forwarding  
11 lookup, and in which accesses to that shared memory are multiplexed and prioritized to  
12 maximize throughput and minimize routing latency.

13

14 Summary of the Invention

15

16 The invention provides a single-chip router. The router includes a memory  
17 shared among packet buffers for receiving packets, packet buffers for transmitting pack-  
18 ets, and packet header buffers for packet forwarding lookup. Accesses to that shared  
19 memory are multiplexed and prioritized. Packet reception is performed with relatively  
20 high priority, packet transmission is performed with medium priority, and packet for-  
21 warding lookup is performed with relatively low priority.

22

23 In a preferred embodiment, the single-chip router includes circuits for seri-  
24 ally receiving packet header information, converting that information into a parallel for-  
25 mat for transmission to an SRAM for lookup, and queuing input packets for later for-

1 warding at an output port. Similarly, in a preferred embodiment, the single-chip router  
2 includes circuits for queuing output packets for transmission at an output port, receiving  
3 packet forwarding information from the SRAM in a parallel format, and converting  
4 packet header information from output packets into a serial format for transmission. The  
5 single-chip router also includes a region in its shared memory for a packet forwarding  
6 table, and circuits for performing forwarding lookup responsive to packet header infor-  
7 mation.

#### 8 9 Brief Description of the Drawings

10  
11 Figure 1 shows a block diagram of a system including a single-chip router.

12  
13 Figure 2 shows a process flow diagram of a method for operating a system  
14 including a single-chip router.

#### 15 16 Detailed Description of the Preferred Embodiment

17  
18 In the following description, a preferred embodiment of the invention is  
19 described with regard to preferred process steps and data structures. Those skilled in the  
20 art would recognize after perusal of this application that embodiments of the invention  
21 can be implemented using circuits adapted to particular process steps and data structures  
22 described herein, and that implementation of the process steps and data structures de-  
23 scribed herein would not require undue experimentation or further invention.

24

1    *System Elements*

2

3            Figure 1 shows a block diagram of a system including a single-chip router.

4

5            A system 100 includes a single-chip router 110, a memory 120 coupled to  
6    the router 110 using a memory bus 121, and a processor 130 coupled to the router 110  
7    using a processor bus 131.

8

9            The router 110 includes a plurality of input ports 111, a plurality of output  
10   ports 112, a memory port 113 coupled to the memory bus 121, a processor port 114 cou-  
11   pled to the processor bus 131, and a set of internal memory and internal processing cir-  
12   cuits integrated into a single monolithic integrated circuit on at least one side of a silicon  
13   die.

14

15           In a preferred embodiment, the memory 120 includes an SRAM, and the  
16   memory bus 130 includes a 256 bit wide bus operating at about 125 megahertz, so as to  
17   provide 32 gigabits per second full duplex communication (that is, both to and from the  
18   memory 120). The memory 120 includes sufficient storage to record a set of packets 140  
19   which are received from the input ports 111 and which are in transit to the output ports  
20   112.

21

22           The memory port 113 includes a memory data register 151 having 64 eight-  
23   bit bytes disposed in a set of four groups of 16 eight-bit bytes, and disposed for receiv-  
24   ing data from selected registers of the memory 120 (such as in memory read operations)  
25   and for transmitting data to selected registers of the memory 120 (such as in memory

1 write operations). The memory port 113 also includes a memory address register 152 for  
2 selecting the registers of the memory 120 to be read or written.

3

#### 4 Packet Receive Circuits

5

6 Each one of the input ports 111 is coupled to an input MAC circuit 161, for  
7 receiving a set of packets 140 from the input port 111, recognizing a MAC address of the  
8 sending device, recognizing a MAC address of the router 110 (as the receiving device),  
9 and coupling the packets 140 to an input packet queue 162. In a preferred embodiment,  
10 the input MAC circuit 161 receives the packets 140 in a bit serial format and outputs  
11 them to the input packet queue 162 as a sequence of eight-bit bytes.

12

13 The input packet queue 162 includes a shift register, for receiving the se-  
14 quence of eight-bit bytes in serial from the input MAC circuit 161, and for transmitting a  
15 set of 256 bits (that is, 64 eight-bit bytes) in parallel to the memory data port 151. In a  
16 preferred embodiment, the input packet queue 162 is double-buffered; that is, it includes  
17 two separate shift registers, one of which can be reading packets 140 in serial from the  
18 input MAC circuit 161 while the other can be writing packets 140 in parallel to the  
19 memory data port 151.

20

21 The input packet queue 162 is coupled to a receive request circuit 163, for  
22 determining that the packet 140 has been received (or partially received, if more than  
23 256 bits in length), and for signalling the memory 120 to read the packet 140 from the  
24 input packet queue 162. The receive request circuit 163 is coupled to the memory ad-  
25 dress register 152 and to a control signal for the memory 120.



1

2 Packet Transmit Circuits

3

4           Similar to the input ports 111, each one of the output ports 112 is coupled  
5 to an output MAC circuit 171, for transmitting a set of packets 140 from the output port  
6 112, adding a MAC address for the router 110 (as the sending device), adding a MAC  
7 address for the receiving device, and coupling the packets 140 from an output packet  
8 queue 172. In a preferred embodiment, the output MAC circuit 161 receives the packets  
9 140 as a sequence of eight-bit bytes and outputs them from the output packet queue  
10 172 in a bit serial format.

11

12           Similar to the input packet queue 162, the output packet queue 172 in-  
13 cludes a shift register, for receiving a set of 256 bits (that is, 64 eight-bit bytes) in parallel  
14 from the memory data port 151, and for transmitting a sequence of eight-bit bytes in se-  
15 rial to the output MAC circuit 171. In a preferred embodiment, the output packet queue  
16 172 is double-buffered; that is, it includes two separate shift registers, one of which can  
17 be reading packets 140 in parallel from the memory data port 151 while the other can be  
18 writing packets 140 in serial to the output MAC circuit 171.

19

20           Similar to the input request circuit 163, the output packet queue 172 is  
21 coupled to a transmit request circuit 173, for determining that the packet 140 is ready to  
22 be transmitted (or partially ready, if more than 256 bits in length), and for signaling the  
23 memory 120 to write the packet 140 to the output packet queue 162. The transmit re-  
24 quest circuit 173 is coupled to the memory address register 152 and to a control signal  
25 for the memory 120.

1

2 Packet Address Lookup Circuits

3

4

5 The input packet queue 162 is also coupled to a packet header queue 182,  
6 for isolating a packet header 141 for the packet 140 and for performing address lookup  
7 for that packet header 141. In a preferred embodiment, the packet header queue 182 re-  
8 ceives the packet header 141 in parallel from the input packet queue 162.

8

9

10 The packet header queue 182 includes a shift register, for receiving a set of  
11 256 bits (that is, 64 eight-bit bytes) in parallel from the input packet queue 162, and for  
12 coupling the packet header 141 to an address request circuit 183. In a preferred em-  
13 bodiment, the packet header queue 182 is double-buffered; that is, it includes two sepa-  
14 rate shift registers, one of which can be reading packet headers 141 in parallel from the  
15 input packet queue 162 while the other can be coupling packet headers 141 to the ad-  
16 dress request circuit 183.

16

17

18 The address request circuit 183 includes a hash circuit 184 for determining  
19 a hash address for packet lookup in the memory 120. The hash circuit 184 is coupled to  
20 the memory address register 152 for supplying a hash address to the memory 120 for per-  
21 forming packet lookup. The address request circuit 183 is also coupled to a control sig-  
22 nal for the memory 120.

22

23

24 In a preferred embodiment, the hash circuit 184 is responsive to a (source,  
25 destination) pair in the packet header 141, such as described in detail in the following  
co-pending patent applications:

1

2 o U.S. Application Serial No. 08/581,134, titled "Method For Traffic Management,  
3 Traffic Prioritization, Access Control, and Packet Forwarding in a Datagram Com-  
4 puter Network", filed December 29, 1995, in the name of inventors David R.  
5 Cheriton and Andreas V. Bechtolsheim, assigned to Cisco Technology, Inc., at-  
6 torney docket number CIS-019;

7

8 o U.S. Application Serial No. 08/655,429, titled "Network Flow Switching and  
9 Flow Data Export", filed May 28, 1996, in the name of inventors Darren Kerr and  
10 Barry Bruins, and assigned to Cisco Technology, Inc., attorney docket number  
11 CIS-016; and

12

13 o U.S. Application Serial No. 08/771,438, titled "Network Flow Switching and  
14 Flow Data-Export", filed December 20, 1996, in the name of inventors Darren  
15 Kerr and Barry Bruins, assigned to Cisco Technology, Inc., attorney docket num-  
16 ber CIS-017.

17

18 These patent applications are collectively referred to herein as the  
19 "Netflow Switching Disclosures". Each of these applications is hereby incorporated by  
20 reference as if fully set forth herein.

21

22 The memory 120 responds to the hash address by delivering a set of  
23 packet lookup information to the memory data register 151, which is coupled to the  
24 packet header queue 182. The address request circuit 183 also includes a comparator

1 185 for determining which of several packet lookup responses coupled to the packet  
2 header queue 182 is associated with the actual packet header 141.

3  
4 The packet header queue 182 is also coupled to the processor bus 131, for  
5 coupling packet headers 141 and packet lookup information to the processor 130 for  
6 extraordinary processing. Thus, when the router 110 is unable to process the packet  
7 140, or processing the packet 140 requires more flexibility than available to the router  
8 110 and the memory 120, the packet header 141 is coupled to the processor 130 for ex-  
9 traordinary processing.

10  
11 In a preferred embodiment, such extraordinary processing can include en-  
12 hanced packet forwarding and traffic management services such as access control, mul-  
13 ticast packet processing, random early discard, and other known packet processing  
14 services.

15

#### 16 *System Operation*

17

18 Figure 2 shows a process flow diagram of a method for operating a system  
19 including a single-chip router.

20

21 A method 200 includes a set of flow points to be noted, and steps to be  
22 executed, cooperatively by the system 100, including the router 110, the memory 120,  
23 and the processor 130.

24

1                   At a flow point 210, an incoming packet 140 is received at one of the input  
2 ports 111.

3

4                   At a step 221, the input MAC circuit 161 receives the packet 140 and both  
5 recognizes the MAC address for the sending device, and confirms that the MAC address  
6 for the receiving device is the router 110.

7

8                   At a step 222, the input packet queue 162 receives the packet 140.

9

10                  At a step 223, the receive request circuit 163 determines a location in the  
11 memory 120 for the packet 140, and signals the memory 120 to receive the packet 140.

12

13                  At a step 224, the packet 140 is read into the shared memory 120 from the  
14 input packet queue 162.

15

16                  At a flow point 230, the packet 140 is ready to be routed.

17

18                  At a step 241, the packet header 141 for the packet 140 is coupled from the  
19 input packet queue 162 to the packet header queue 182.

20

21                  At a step 242, the hash circuit 184 determines a hash address for the  
22 (source, destination) pair in the packet header 141, as described in the Netflow Switch-  
23 ing Disclosures, hereby incorporated by reference.

24

1           At a step 243, the address request circuit 163 couples the packet header  
2   151 to the memory data register 151, couples the hash address to the memory address  
3   register 152, and signals the memory 120 to perform a packet address lookup.  
4

5           At a step 244, the memory 120 performs the packet address lookup and  
6   returns its packet lookup results to the memory data register 151. In a preferred em-  
7   bodiment, the memory 120 is disposed as a four-way set-associative memory responsive  
8   to the hash address provided by the hash circuit 184, so there are four packet lookup  
9   results.  
10

11           At a step 245, the comparator 185 determines which one of the four packet  
12   lookup results is valid for the (source, destination) pair in the packet header 141, and se-  
13   lects that one of the four packet lookup results for packet forwarding.  
14

15           At a flow point 250, the packet 140 is ready to be transmitted in response  
16   to the packet lookup results.  
17

18           At a step 261, the transmit request circuit 173 determines the location in  
19   the memory 120 for the packet 140, and signals the memory 120 to transmit the packet  
20   140.  
21

22           At a step 262, the packet 140 is read from the shared memory 120 into the  
23   transmit packet queue 172.  
24

1           At a step 263, the output MAC circuit 171 both recognizes the MAC ad-  
2      dress for the sending device, and adds the MAC address for the receiving device (the  
3      router 110 itself), and transmits the outgoing packet 140 on the output port 112.

4  
5           At a flow point 270, an outgoing packet has been transmitted at one of the  
6      output ports 112.

7  
8           The router 110 operates with regard to each packet 140 using a parallel  
9      pipeline. Thus, a first packet 140 is being received while a second packet is being trans-  
10     mitted while a third packet 140 is having a packet lookup performed.

11  
12          The memory 120 has two regions (a packet buffer region for incoming and  
13      outgoing packets 140, and a packet header region for packet header lookup), each of  
14      which is intended to be accessed rapidly and often. However, multiple accesses to the  
15      memory 120 do not occur simultaneously; instead they are multiplexed so that accesses  
16      to these regions are each serviced often by the memory 120, and prioritized so that ac-  
17      cesses to these regions can each be serviced rapidly by the router 110.

18  
19          In a preferred embodiment, packet reception is performed with relatively  
20      high priority, packet transmission is performed with medium priority, and packet for-  
21      warding lookup is performed with relatively low priority.

22  
23          Access requests by the receive request circuit 163 have the highest prior-  
24      ity, so that when requests for such accesses are received by the memory 120, they are  
25      processed before requests for accesses by other circuits. Thus, incoming packets are en-

1    tered into and retrieved from the input packet queue 162 as quickly as possible, so that  
2    queuing at the input ports 111 of the router 110 is minimized.

3  
4           Access requests by the transmit request circuit 173 have medium priority  
5    (after requests by the receive request circuit 163 and before requests by the address re-  
6    quest circuit 183), so that when requests for such accesses are received by the memory  
7    120, they are processed after requests for accesses by the receive request circuit 163 and  
8    before requests by the address request circuit 183. Thus, outgoing packets are entered  
9    into and retrieved from the output packet queue 172 as quickly as possible after incom-  
10   ing packets are processed.

11  
12           Access requests by the address request circuit 183 have the lowest priority,  
13    so that when requests for such accesses are received by the memory 120, they are proc-  
14   essed after requests for access by other circuits.

15  
16    *Alternative Embodiments*

17  
18           Although preferred embodiments are disclosed herein, many variations are  
19    possible which remain within the concept, scope, and spirit of the invention, and these  
20    variations would become clear to those skilled in the art after perusal of this application.

21



Claims

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2

3

1. A router, including

4

at least one port disposed for receiving packets;

5

at least one port disposed for transmitting packets; and

6

processing circuits integrated into a single monolithic integrated circuit on

7

at least one side of a silicon die, said processing circuits including

8

means for accessing a shared memory, said means including (a) circuits dis-

9

posed for copying packets between at least one region of said shared memory and said

10

processing circuits, and (b) circuits disposed for performing packet lookup in at least one

11

region of said shared memory, said packet lookup being responsive to packet headers of

12

said packets.

13

14

2. A router as in claim 1, wherein said at least one port disposed for re-

15

ceiving packets includes a plurality of ports disposed for receiving packets.

16

17

3. A router as in claim 1, wherein said at least one port disposed for

18

transmitting packets includes a plurality of ports disposed for transmitting packets.

19

20

4. A router as in claim 1, wherein said circuits disposed for copying

21

packets include circuits for receiving packet information in a parallel format and con-

22

verting that information into a serial format.

23

1           5.     A router as in claim 1, wherein said circuits disposed for copying  
2     packets include circuits for receiving packet information in a serial format and convert-  
3     ing that information into a parallel format.

4  
5           6.     A router as in claim 1, wherein said means for accessing said shared  
6     memory includes circuits disposed for multiplexing and prioritizing requests for copying  
7     incoming packets to said shared memory, requests for copying outgoing packets from  
8     said shared memory, and requests for performing packet lookup.

9  
10          7.     A router as in claim 6, wherein said circuits disposed for multiplex-  
11     ing and prioritizing assign relatively high priority to said requests for copying incoming  
12     packets to said shared memory.

13  
14          8.     A router as in claim 6, wherein said circuits disposed for multiplex-  
15     ing and prioritizing assign relatively low priority to said requests for copying outgoing  
16     packets from said shared memory.

17  
18          9.     A router as in claim 6, wherein said circuits disposed for multiplex-  
19     ing and prioritizing assign priority to said requests in a manner so as to maximize  
20     throughput and minimize routing latency.

21  
22          10.    Apparatus including  
23                a shared memory, said shared memory including packet buffers for packets  
24     and packet lookup information;

1 a router coupled to said shared memory, said router including processing  
2 circuits integrated into a single monolithic integrated circuit on at least one side of a sili-  
3 con die, said processing circuits including

4 means for accessing said shared memory, said means including (a) circuits  
5 disposed for copying packets between at least one region of said shared memory and  
6 said processing circuits, and (b) circuits disposed for accessing said shared memory for  
7 performing packet lookup.

8

9 11. Apparatus as in claim 10, including a processor coupled to said  
10 router.

11

12 12. Apparatus as in claim 10, wherein said means for accessing said  
13 shared memory includes circuits disposed for multiplexing and prioritizing requests for  
14 copying incoming packets to said shared memory, requests for copying outgoing pack-  
15 ets from said shared memory, and requests for performing packet lookup.

16

17 13. Apparatus as in claim 12, wherein said circuits disposed for multi-  
18 plexing and prioritizing assign relatively high priority to said requests for copying in-  
19 coming packets to said shared memory.

20

21 14. Apparatus as in claim 12, wherein said circuits disposed for multi-  
22 plexing and prioritizing assign relatively low priority to said requests for copying out-  
23 going packets from said shared memory.

24

1           15. Apparatus as in claim 12, wherein said circuits disposed for multi-  
2     plexing and prioritizing assign priority to said requests in a manner so as to maximize  
3     throughput and minimize routing latency.

4  
5           16. Apparatus as in claim 12, wherein said circuits disposed for copying  
6     packets include circuits for receiving packet information in a parallel format and con-  
7     verting that information into a serial format.

8  
9           17. Apparatus as in claim 12, wherein said circuits disposed for copying  
10    packets include circuits for receiving packet information in a serial format and convert-  
11    ing that information into a parallel format.

12  
13          18. A method, including the steps of  
14          receiving packets using at least one input port;  
15          transmitting packets using at least one output port; and  
16          routing said packets from said at least one input port to said at least one  
17    output port, using processing circuits integrated into a single monolithic integrated cir-  
18    cuit on at least one side of a silicon die.

19  
20          19. A method, including the steps of  
21          receiving packets using at least one input port;  
22          transmitting packets using at least one output port;  
23          copying packets between at least one region of a shared memory and a set  
24    of processing circuits integrated into a single monolithic integrated circuit on at least one  
25    side of a silicon die; and

1 performing packet lookup using said shared memory and said processing  
2 circuits.

3  
4 20. A method as in claim 19, wherein said at least one input port in-  
5 cludes a plurality of ports disposed for receiving packets.

6  
7 21. A method as in claim 19, wherein said at least one output port in-  
8 cludes a plurality of ports disposed for transmitting packets.

9  
10 22. A method as in claim 19, wherein said step of copying packets in-  
11 cludes the steps of receiving packet information in a parallel format and converting that  
12 information into a serial format.

13  
14 23. A method as in claim 19, wherein said step of copying packets in-  
15 cludes the steps of receiving packet information in a serial format and converting that  
16 information into a parallel format.

17  
18 24. A method as in claim 19, wherein said steps of copying packets and  
19 performing packet lookup include the steps of multiplexing and prioritizing requests for  
20 copying incoming packets to said shared memory, requests for copying outgoing pack-  
21 ets from said shared memory, and requests for performing packet lookup.

22  
23 25. A method as in claim 24, wherein said steps of multiplexing and pri-  
24 oritizing assign relatively high priority to said requests for copying incoming packets to  
25 said shared memory.

1

2                   26. A method as in claim 24, wherein said steps of multiplexing and pri-  
3     oritizing assign relatively low priority to said requests for copying outgoing packets  
4     from said shared memory.

5

6                   27. A method as in claim 24, wherein said steps of multiplexing and pri-  
7     oritizing assign priority to said requests in a manner so as to maximize throughput and  
8     minimize routing latency.

9

10                  28. A method, including the steps of  
11                    recording packets and packet lookup information in a shared memory;  
12                    coupling processing circuits to said shared memory, said processing circuits  
13     being integrated into a single monolithic integrated circuit on at least one side of a sili-  
14     con die, said processing circuits including (a) circuits disposed for copying packets be-  
15     tween at least one region of said shared memory and said processing circuits, and (b) cir-  
16     cuits disposed for accessing said shared memory for performing packet lookup.

17

18                  29. A method, including the steps of  
19                    recording packets and packet lookup information in a shared memory;  
20                    copying packets between at least one region of said shared memory, and  
21     accessing said shared memory to perform packet lookup, using processing circuits which  
22     are integrated into a single monolithic integrated circuit on at least one side of a silicon  
23     die.

24

1           30. A method as in claim 29, including coupling a processor to said  
2 processing circuits.

3  
4           31. A method as in claim 29, wherein said steps of copying packets and  
5 accessing said shared memory include the steps of multiplexing and prioritizing requests  
6 for copying incoming packets to said shared memory, requests for copying outgoing  
7 packets from said shared memory, and requests for performing packet lookup.

8  
9           32. A method as in claim 31, wherein said steps of multiplexing and pri-  
10 oritizing assign relatively high priority to said requests for copying incoming packets to  
11 said shared memory.

12  
13           33. A method as in claim 31, wherein said steps of multiplexing and pri-  
14 oritizing assign relatively low priority to said requests for copying outgoing packets  
15 from said shared memory.

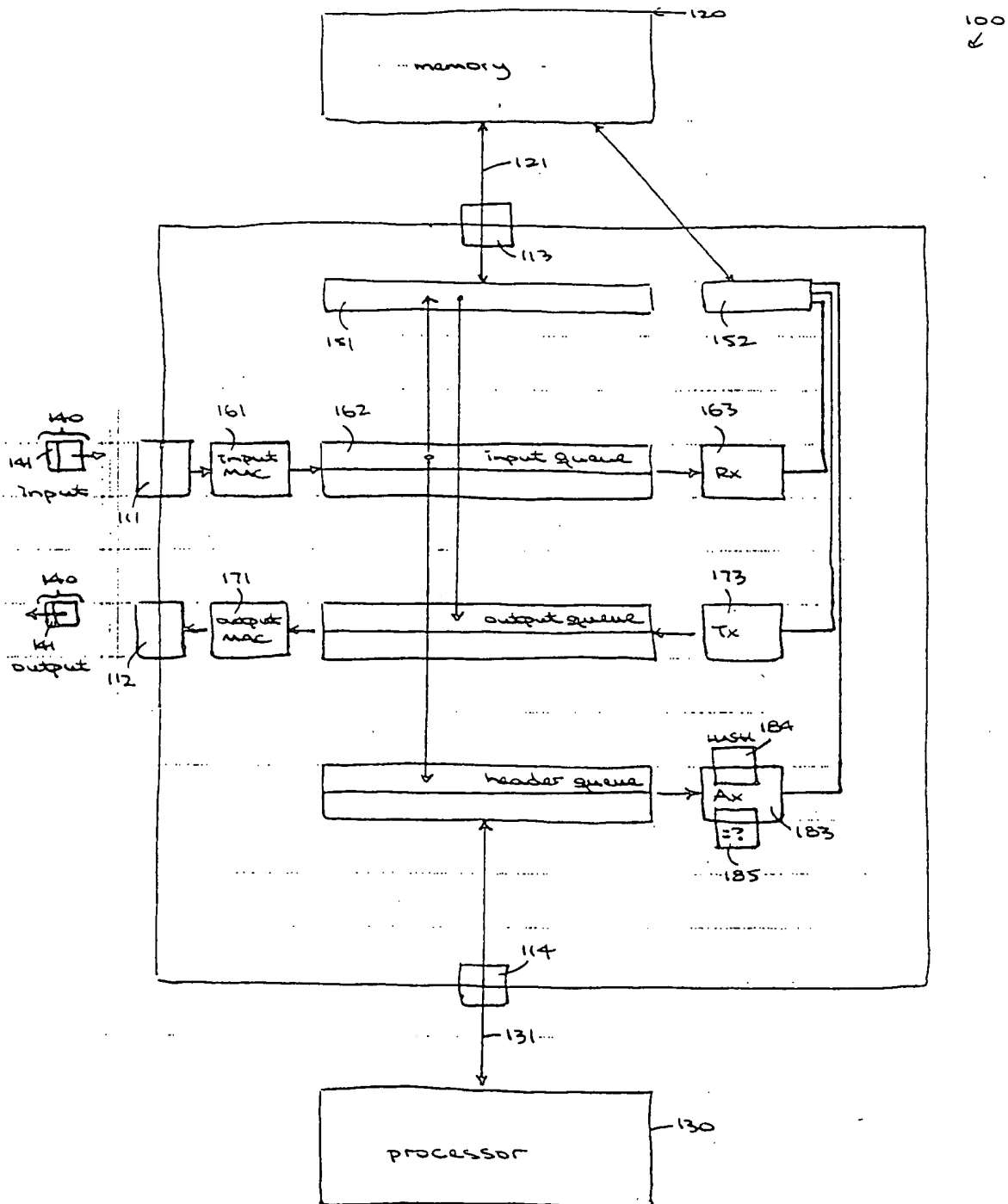
16  
17           34. A method as in claim 31, wherein said steps of multiplexing and pri-  
18 oritizing assign priority to said requests in a manner so as to maximize throughput and  
19 minimize routing latency.

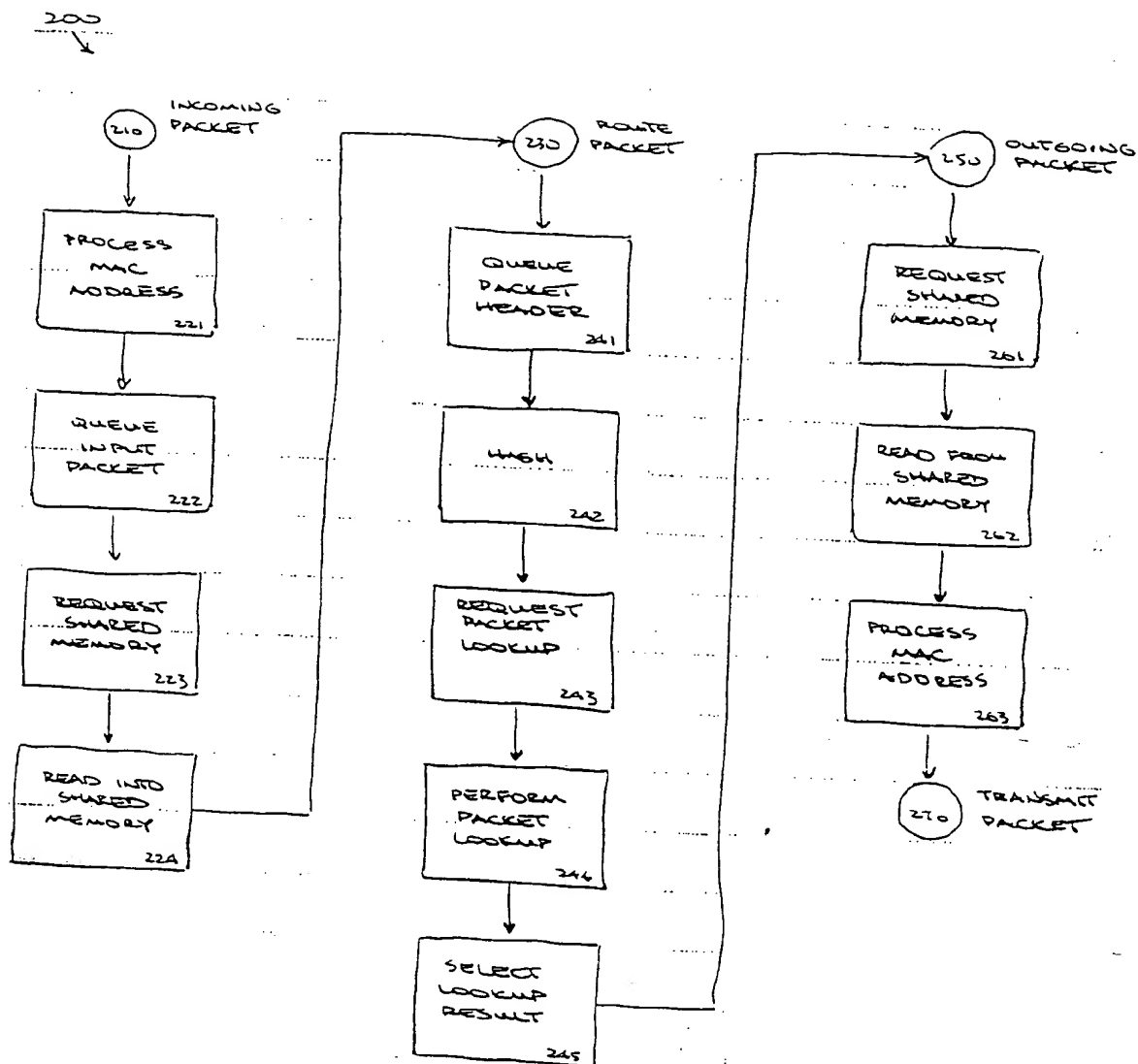
20  
21           35. A method as in claim 31, wherein said steps of copying packets in-  
22 clude the steps of receiving packet information in a parallel format and converting that  
23 information into a serial format.

24

- 1                   36. A method as in claim 31, wherein said steps of copying packets in-  
2     clude the steps of receiving packet information in a serial format and converting that in-  
3     formation into a parallel format.  
4







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